**IN THE CLAIMS:**

Please amend Claim 1 and Claim 9 as follows:

1. (Twice amended) A method of improving the SiGe bipolar yield of a SiGe heterojunction bipolar transistor comprising the steps of:

providing a heterojunction bipolar transistor structure comprising at least an underlying SiGe base region, an insulator layer formed on surface portions of said underlying SiGe base region, and an emitter formed on said insulator layer and in contact with said underlying SiGe base region through an emitter opening formed in said insulator layer, said emitter, said insulator layer and said SiGe base region each having exposed sidewalls;

forming a permanent passivation layer on said exposed sidewalls of said emitter, said insulator layer and portions of said SiGe base region; and

siliciding exposed silicon surfaces of at least said emitter and said SiGe base region not protected by said permanent passivation layer to form silicide regions therein.

9. (Three times amended) A SiGe heterojunction bipolar transistor comprising:

a semiconductor substrate having a collector and subcollector region located therein, wherein said collector is located between isolation regions that are also present in the substrate;

a SiGe layer atop said substrate, said SiGe layer including polycrystalline Si regions positioned above said isolation regions and a SiGe base region located above said collector and subcollector regions;

a patterned insulator layer atop said SiGe base region, said patterned insulator having an opening therein;

an emitter located on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter, said patterned insulator layer and said SiGe base region each having exposed sidewalls;

a permanent conformal passivation layer positioned on said exposed sidewalls of said emitter, said patterned insulator layer and a portion of said SiGe base region; and

silicide regions located on exposed portions of said SiGe layer, including portions of said SiGe base region, and said emitter not covered by said permanent conformal passivation layer.

Please add new Claim:

--18. A SiGe heterojunction bipolar transistor comprising:

a semiconductor substrate having a collector and subcollector region located therein, wherein said collector is located between isolation regions that are also present in the substrate;

a SiGe layer atop said substrate, said SiGe layer including polycrystalline Si regions positioned above said isolation regions and a SiGe base region located above said collector and subcollector regions;

a patterned insulator layer atop said SiGe base region, said patterned insulator having an opening therein;

an emitter located on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter, said patterned insulator layer and said SiGe base region each having exposed sidewalls;

a permanent conformal passivation layer positioned on said exposed sidewalls of said emitter, said patterned insulator layer and an inclined portion of said SiGe base region; and

silicide regions located on exposed portions of said SiGe layer, including portions of said SiGe base region, and said emitter not covered by said permanent conformal passivation layer.--

## REMARKS

Favorable reconsideration and allowance of the claims of the present application, as amended herein, are respectfully requested.

Before addressing the specific rejection raised in the Final Rejection dated October 15, 2002, applicants have amended Claim 1 and Claim 9, and added new Claim 18. Claims 1 and 9 are amended to positively recite that the passivation layer is a "permanent" component of the claimed SiGe heterojunction bipolar transistor. Support for the amendments to Claims 1 and 9 is found throughout the present specification; i.e., FIG. 2, FIG. 8, and Page 5, line 30 – Page 6, line 5. Specifically, referring to Page 5, line 32 – Page 6, line 1, the "passivation layer **68** prevents bridging between adjacent silicide